DS-02-017

February 5, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/615,124 07/08/03

Horst Knoedgen

NATURAL ANALOG OR MULTILEVEL TRANSISTOR DRAM-CELL

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 17, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 2/17/04

U.S. Patent 4,694,341 to Soneda et al., "Sample-and-hold Circuit," discusses a sample-and-hold circuit adapted for a video signal or the like having a blanking period per pre-determined cycle.

U.S. Patent 5,500,522 to Eshraghian et al., "Gallium Arsenide MESFET Imager," discusses a photoresponsive device based on Gallium Arsenide (GaAs) Integrated Circuit (IC) MESFET technology.

International Patent Application WO 86/07488 to Buchele, "Fast-in-slow-out (FISO) Sampling Systems," discusses a fast-in, slow-out sampling system that operates at a very high sampling frequencay at high accuracy.

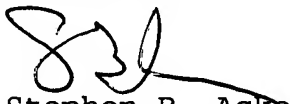
European Patent Application 0 442 335 A1 to Uemura et al., "Semiconductor Memory Device Including Nonvolatile Memory Cells, Enhancement Type Load Transistors, and Peripheral Circuits Having Enhancement Type Transistors," discloses a semiconductor memory devcie including nonolatile memory cell transistors.

U.S. Patent Application Publication US 2002/0167845 A1 to Jain, "Reducing Leakage Current in Memory Cells," discloses a memory cell having first and second access transistors coupled to a storage transistor.

U.S. Patent Application Publication US 2003/0090948 A1 to Kanno et al., "Semiconductor Device Having Memory Cells Coupled to Read and Write Data Lines," discloses a technique for mounting a large-capacity memory and a logic circuit on the same chip.

U.S. Patent 3,760,380 to Hoffman et al., "Silicon Gate Complementary MOS Dynamic RAM," discusses monolithic integrated circuit dynamic random access memory (RAM) systems using enhancement mode field effect transistors.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
DS-02-017	10/615,124
Applicant: Horst Knoedgen	
Filing Date: 07/08/03	Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4694341	9/15/87	Soneda et al.	358	160	2/4/86
	5500522	3/19/96	Eshraghian et al.	250	208.1	4/15/93
	3760380	9/18/73	Hoffman et al.	340	173R	6/2/72

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
WO	86/07488	12/18/86	Int'l Patent App.	G11C	27/02		
EP	0442335A1	8/21/91	European Patent App.	G11C	16/04		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- U.S. Patent App. Pub. US 2003/0090948 A1, Kanno et al., Pub. Date 5/15/03, U.S. Class 365/200, Filed 12/23/02.
- U.S. Patent App. Pub. US 2002/0167845 A1 to Jain, Pub. Date 11/14/02, US Class 365/187, Filed 5/14/01.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.